REMARKS

The Applicants respectfully request further examination and consideration in view of the above amendments and the arguments set forth fully below. Claims 1-5 were previously pending in this application. Within the Office Action, Claims 1-5 stand rejected. By the above amendments, Claims 1, 2, 4 and 5 have been amended, Claim 6-16 have been added, and no claims have been canceled. Accordingly, Claims 1-16 are currently pending. No new matter has been added by this amendment.

Request for Consideration of Pending Information Disclosure Statements

On March 28, 2005, the Examiner initialed some, but not all, of the cited documents listed on three Supplemental IDS mailed October 17, 2003, November 17, 2003, and November 17, 2004. Instead, the cited documents were crossed out for nonconformance and further as an indication that the documents were not considered.

Specifically, one Japanese patent (Japan Patent No. 63-155248) is listed on the Supplemental IDS mailed October 17, 2003, but it was crossed out by the Examiner. Four Japanese patents (Japan Patent No. 10-79197, Japan Patent No. 9-147581, Japan Patent No. 5-46461, and Japan Patent No. 5-233426) are listed on the Supplemental IDS mailed November 17, 2003, but they too were crossed out by the Examiner. Finally, two Japanese patents (Japan Patent No. 5-282883 and Japan Patent No. 7-122092) are listed on the Supplemental IDS mailed November 17, 2004, but they also were crossed out by the Examiner.

Pursuant to 37 CFR 1.98(a)(3), abstracts in English for these seven Japanese patents are attached hereto in the **Appendix**. The Applicants respectfully request that the Examiner consider these seven Japanese patents and indicate this on the appropriate PTO Form 1449.

Rejection under 35 U.S.C. § 102(e)

The independent claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Jones, U.S. Patent No. 5,928,347 (hereinafter, "Jones"). Within the Office Action, it is stated that Jones teaches a flash memory card interfacing system (interface apparatus 10 of Figs. 2 and 3) for detachably coupling to a host computer system (host computer 156 of Fig. 3), the flash memory card interface system also configured for performing data storage and control operations

(col. 5 lines 16-50), the flash memory card interfacing system comprising: a device (USB interface 144) for connecting a flash memory card (ATA memory card 62) to a USB port (connector 140). The Applicants respectfully traverse this rejection.

Jones discloses a removable memory card interface apparatus which enables a removable memory card to communicate with a number of peripheral devices directly without the need for the memory card's host or a host computer. The interface apparatus includes a micro-controller operating with an internal bus to control, process and route signals between the removable memory and a peripheral device via a series of memory and device interfaces. A control panel and/or remote control allows a user to interact with the interface apparatus. In one embodiment, the interface apparatus also allows a host computer to communicate with the memory card via one of the peripheral device ports. [Abstract]

The independent claim 1 is directed to a flash memory card interfacing system for detachably coupling to a host computer system, the flash memory card interfacing system also configured for performing data storage and control operations, the flash memory card interfacing system comprising: a device for connecting a flash memory card to a USB port, ***such that the flash memory card operates as a removable data storage for the host computer system*** (emphasis added). Jones does not teach all the limitations found in the independent claim 1.

Specifically, **Jones does <u>not</u> teach that the flash memory card of the interface system operates as a removable data storage for the host computer.** Instead, **in Jones, "[d]ata transferred between a memory device and a peripheral device is buffered and cached in RAM 36."** [Jones, col. 5, lines 49-50 and Fig. 2]. **Unlike Jones, the present invention does <u>not</u> require that data be buffered and cached in the interface.** The present invention discloses a flash memory card interfacing system comprising a device for connecting a flash memory card to a USB port, such that the flash memory card operates as a removable data storage for the host computer system without the need for external caching. The interfacing system of the present invention allows for the **<u>direct</u>** transfer of data between the flash memory card and the host computer system, thereby eliminating the need for external caching. For at least these reasons, the independent Claim 1 is allowable over the teachings of Jones.

Rejections under 35 U.S.C. § 103(a)

Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Shahar et al, U.S. Patent No. 5,922,055 (hereinafter, "Shahar"). Further, claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Jones and Shahar in view of Jigour et al, U.S. Patent No. 5,877,975 (hereinafter, "Jigour").

Specifically, as to independent claim 2, it is stated within the Office Action that

> . . . Shahar teaches a flash memory card interfacing system (Plug and Play card 1 of fig. 4) for coupling a flash memory device (EEPROM 3 wherein the EEPROM 3 is access programmable non-volatile memory device) to a signal line 9 (fig. 4), the flash memory card interfacing system comprising:
>
> a. a flash memory module (EEPROM 3) for executing a write operation, a read operation, and an erase operation (col. 5 line 24 to col. 6 line 13);
>
> b. an interface device (micro controller 2) for coupling the flash memory card to a ISA port (it is inherently a standard ISA Plug and Play interface 4 has an ISA port);
>
> c. a standard ISA Plug and Play interface 4 (fig. 4) for connecting the signal line 9, sending and receiving signals, and coupling the interface device to the flash memory card (col. 5 lines 23-50);
>
> d. a flash controller (Plug and Play controller 8 of fig. 4) coupled to the flash memory module and the ISA PnP interface 4, the flash controller controlling the ISA PnP interface 4 and configuring the flash memory card to a selected operating mode of the interface device (col. 5 line 31 to col. 6 line 13); and
>
> f. flash interface circuitry (logic circuitry 14 of fig. 4) coupled to the controller, the flash interface circuitry identifying the selected operating mode of the interface device (col. 6 line 66 to col. 7 line 10).
>
> Although Shahar teaches substantial features (discussed above), he fails to explicitly teach a USB bus, a USB port and a USB connector. Jones; however, teaches the USB bus, the USB port and the USB connector (connector 140 and USB interface 144 of figs 2 and 3). It would have been obvious to a person of ordinary skill in the art to have the USB interface in order to provide high data transfer rate, connecting up 127 devices and Plug and Play installation.

[Office Action mailed March 31, 2005 (hereinafter, "Office Action"), pages 3 and 4] The Applicants respectfully traverse this rejection.

Shahar discloses that in a Plug and Play environment, different kinds of EEPROMs can be used having different access protocols without having to add an additional pin to the EEPROM to indicate its type. The first type of EEPROM has a code which indicates the first

type stored on a predetermined address whereas the second type of EEPROM having a different read protocol has another code which indicates the second type stored on a consecutive address. When the Plug and Play controller accesses the EEPROM for a read either the code 1 or code 2 is outputted whereby the appropriate read protocol is identified. [Abstract]

Jones discloses a removable memory card interface apparatus which enables a removable memory card to communicate with a number of peripheral devices directly without the need for the memory card's host or a host computer. The interface apparatus includes a micro-controller operating with an internal bus to control, process and route signals between the removable memory and a peripheral device via a series of memory and device interfaces. A control panel and/or remote control allows a user to interact with the interface apparatus. In one embodiment, the interface apparatus also allows a host computer to communicate with the memory card via one of the peripheral device ports. [Abstract]

Neither Shahar, Jones, nor the combination of Shahar and Jones teach all the limitations found in the independent claim 2. Specifically, neither Shahar, Jones, nor the combination of Shahar and Jones teach a flash controller coupled to the flash memory module and the USB connector, *the flash controller controlling the USB connector and configuring the flash memory card to a selected operating mode of the interface device.* (emphasis added) Further, neither Shahar, Jones, nor the combination of Shahar and Jones teach a flash interface circuitry coupled to the flash controller, *the flash interface circuitry identifying the selected operating mode of the interface device.* (emphasis added)

According to the Office Action, Shahar teaches a flash controller (Plug and Play controller 8 of fig. 4) that configures a flash memory card (EEPROM 3) to a selected operating mode of the interface device (citing col. 5 line 31 to col. 6 line 13). [Office Action, pages 3-4] The Office Action further identifies the interface device in Shahar as the micro controller 2 in Fig. 4. [Office Action, page 3]. However, **Shahar fails to provide a teaching, disclosure, or suggestion that a flash controller configures the flash memory card to a selected operating mode of the interface device.**

First, the Applicants disagree with the characterizations of the Plug and Play controller 8 of Fig. 4 as a flash controller, the EEPROM 3 as a flash memory card, and the micro controller 2 in Fig. 4 as the interface device. Second, assuming *arguendo* that the characterizations provided in the Office Action are correct, nowhere in Shahar is there a teaching, disclosure, or suggestion, including the cited passage in the Office Action of col. 5 line 31 to col 6 line 13, that the flash

controller (Plug and Play controller 8) configures a flash memory card to a selected operating mode of the interface device (micro controller 2 in Fig. 4). Shahar states that "[t]he Plug and Play controller 8 can deal with 3 different types of read protocols to access the EEPROM 3. . . When the Plug and Play controller 8 needs to read the resource data that is stored in the EEPROM 3 during the Plug and Play procedure first the type of the EEPROM 3 has to be determined for a proper read operation." (col. 5, lines 45-46 and col. 6, lines 1-4). However, Shahar does not teach that a flash controller configures a flash memory card *to a selected operation mode of an interface device* (micro controller 2 in Fig. 4).

Also, the teachings of Shahar are not applicable to flash memory devices. Shahar is directed to serial EEPROM that is not flash memory. "Typically EEPROMs are used in electronic devices for storage of essential information which has to be maintained during power of and/or which has to be available when the electronic system is initialized. One difficulty which is encountered in the usage of such EEPROMs is that there are different types of EEPROMs which have different read protocols. . . This disadvantage is accepted in the prior art in view of the main advantage of a serial EEPROM which is its low cost and small chip size ***as compared to*** parallel non-volatile devices such as ***flash memory devices***." (Shahar, col. 1, lines 18-33) (emphasis added).

Further, Jones does not teach, disclose nor suggest a flash controller configuring a flash memory card to a selected operating mode of the interface device. Jones teaches that a USB interface 144 translates signals between the internal bus 20 and the USB peripheral device 142 [col. 7, lines 33-34], but Jones does not teach, disclose, nor suggest a flash controller configuring a flash memory card to a selected operating mode of the interface device. Further, neither Shahar, Jones, nor the combination of Shahar and Jones teach a flash interface circuitry coupled to the flash controller, *the flash interface circuitry identifying the selected operating mode of the interface device.* Contrary to what is stated in the Office Action, in Shahar, the flash interface circuitry (characterized as a logic circuitry 14 of Fig. 4) does not identify the selected operating mode of the interface device (micro controller 2). Instead, the logic circuitry 14 controls a comparator 15, which compares a data word received from the EEPROM 3 with codes stored in registers 16, 17, and 18 (Shahar, col. 6, line 66 to col. 7, line 2). Nowhere in Shahar is there a disclosure, teaching, or a suggestion of flash interface circuitry identifying a selected operating mode of an interface device. Further, Jones does not teach, disclosure nor suggest a flash

interface circuitry identifying a selected operating mode of an interface device. For at least these reasons, the independent Claim 2 is allowable over the teachings of Jones in view of Shahar.

Claims 3-5 are dependent upon the independent Claim 2. As discussed above, the independent Claim 2 is allowable over the teachings of Jones in view of Shahar. Accordingly, Claims 3-5 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

New Claims 6-16

Claims 6-15 are new and are in condition of allowance. Claims 6-8 are dependent upon the independent Claim 2. As discussed in the previous section, the independent Claim 2 is allowable over the teachings of Jones in view of Shahar. Accordingly, Claims 6-8 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

The independent claim 9 is directed to a flash memory card interfacing system for detachably coupling to a host computer system, the flash memory card interfacing system also configured for performing data storage and control operations, the flash memory card interfacing system comprising: a device for connecting a flash memory card to a USB port, such that the flash memory card automatically configures itself to cooperatively operate in a selected operating mode through the device. **Neither Jones, Shahar, nor the combination of the two teach all the limitations found in the independent claim 9.**

Claims 10-13 are dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Jones in view of Shahar. Accordingly, Claims 10-13 are also allowable as being dependent on an allowable base claim.

The new independent claim 14 is directed to a flash memory card interfacing system for coupling a flash memory card to a USB bus, the flash memory card interfacing system comprising: (a) the flash memory card for executing a write operation, a read operation, and an erase operation and comprising: an interface device for coupling the flash memory card to a USB port; a flash controller coupled to the flash memory module and a USB connector, the flash controller controlling the USB connector and configuring the flash memory card to a universal serial bus mode of the interface device; and flash interface circuitry coupled to the flash controller, the flash interface circuitry identifying the universal serial bus mode of the interface device; and (b) the USB connector for connecting to the USB bus, sending and receiving signals,

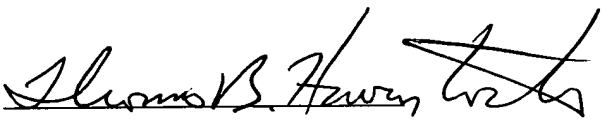
and coupling the interface device to the flash memory card.. **Neither Jones, Shahar, nor the combination of the two teach all the limitations found in the independent claim 14.**

Claims 15 and 16 are dependent on the independent Claim 14. As described above, the independent Claim 14 is allowable over the teachings of Jones in view of Shahar. Accordingly, Claims 15 and 16 are also allowable as being dependent on an allowable base claim.

Conclusion

For the reasons given above, Applicant respectfully submits that Claims 1-16 are in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 6-6-05 By: 

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

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